# DUAL FREQUENCY RF MATCH

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of United States Provisional Application No. 60/530,807 filed December 18, 2003, which is hereby incorporated by reference in its entirety.

## BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention generally relates to semiconductor substrate processing systems and, more particularly, to matching circuits for matching the impedance of a plurality of RF sources coupled to a single electrode to the impedance of a plasma.

Description of the Related Art

[0003] Plasma enhanced semiconductor processing chambers are widely used in the manufacture of integrated devices. In most plasma enhanced semiconductor chambers, multiple radio frequency (RF) generators are utilized to form and control the plasma. Some plasma enhanced processing chambers feed RF power from multiple sources to a single electrode that couples the power to the plasma. However, in those embodiments, each RF source generally requires separate feed structures (*e.g.*, separate RF generator, match output, coaxial cables to the electrode, and the like).

[0004] Therefore, there is a need for an improved apparatus for semiconductor substrate processing that utilizes a single feed structure to couple RF power from multiple RF sources to an electrode.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0005] So that the manner in which the above recited features, advantages and objects of the present invention are attained and can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to the embodiments thereof which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings

illustrate only typical embodiments of this invention and are therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0006] Figure 1 depicts an exemplary block diagram of the RF structure of the present invention;

[0007] Figure 2 is a schematic diagram of one embodiment of the matching circuit of the present invention;

[0008] Figure 3A is a graph depicting the tune space shifting due to shunt variation of complimentary frequency elements;

[0009] Figure 3B is a graph depicting the tune space shifting due to series component variation of complimentary frequency elements;

[0010] Figure 4 is a graph of the tune space of the variable shunt matching circuit of the present invention; and

[0011] Figure 5 is an illustrative schematic diagram of a plasma enhanced processing chamber having one embodiment of a dual frequency matching circuit.

[0012] To facilitate understanding, identical reference numerals have been used, where possible, to designate identical elements that are common to the figures.

## DETAILED DESCRIPTION

[0013] The present invention generally relates to semiconductor substrate processing in a plasma enhanced semiconductor processing chamber. More specifically, the present invention is a dual frequency, variable shunt matching circuit for coupling two RF sources through a single feed to an electrode in a plasma enhanced semiconductor processing chamber.

[0014] Figure 1 depicts a simplified block diagram of a plasma enhanced semiconductor processing chamber having a dual frequency, variable shunt matching circuit. A plasma enhanced processing chamber 100 according to the present invention includes a chamber 102, two RF power sources 104, 106 and a dual frequency matching circuit 108. The chamber 102 includes a powered electrode 110 and a grounded electrode 112. A single feed line 114 from the dual frequency matching circuit 108 electrically couples the sources 104, 106 to

the powered electrode 110. The chamber 102 is otherwise similar to a conventional plasma enhanced processing chamber.

**[0015]** The RF sources 104, 106 are independent, frequency-tuned RF generators. The RF sources 104, 106 may be configured to provide RF power to the chamber 102 in any desired frequency to control characteristics of the plasma. Both frequencies may be selected to control the same plasma characteristic or, alternatively, to control different plasma characteristics. For example, in one embodiment, one of the RF sources 104, 106 is capable of providing high frequency power to excite the plasma and dissociate ions in the plasma and the other one of the RF sources 104, 406 is capable of providing low frequency power to modulate the plasma sheath voltage. For example, in one embodiment, the source 104 may be generally capable of generating a frequency in the range of from about 12.8MHz to about 14.3MHz at up to 5000W of either continuous or pulsed power. The source 106 may be generally capable of generating a frequency in the range of from about 1.8MHz to about 2.2MHz at up to 5000W of either continuous or pulsed power. It is contemplated that other frequencies may be employed.

**[0016]** The dual frequency matching circuit 108 generally includes two matching sub-circuits in which the series elements are fixed and in which the shunt elements provide a variable impedance to ground. The matching circuit 108 includes two inputs that are connected to independent frequency tuned RF power sources 104, 106 at two separate frequencies and provides a common RF output to the processing chamber 102. The matching circuit 108 operates to match the impedance of the sources 104, 106 (typically 50Ω) to that of the processing chamber 102. In one embodiment, the two match sub-circuits are L-type circuits, however, other common match circuit configurations, such as π and T types can be employed.

**[0017]** Figure 2 is a representative circuit diagram of one embodiment of a dual frequency matching circuit 108 having dual L-type match topography. The matching circuit 108 generally includes a low frequency (first) tuning sub-circuit 202, a high frequency (second) tuning sub-circuit 204, and a generator isolation sub-circuit 206. First sub-circuit 202 comprises variable capacitor $C_1$, inductor $L_1$ and capacitor $C_2$. The variable capacitor $C_1$ is shunted across the input

terminals 210A, 210B from the 2MHz source and the inductor $L_1$ and capacitor $C_2$ are connected in series from the input terminals 210A and 210B to the common output terminal 212. In one embodiment, variable capacitor $C_1$ is nominally variable from about 300pF to about 1500pF, inductor $L_1$ is about 30μH, and capacitor $C_2$ is about 300pF.

**[0018]** The generator isolation sub-circuit 206 comprises a ladder topology having three inductors $L_3$, $L_4$ and $L_5$ and three capacitors $C_5$, $C_6$ and $C_7$. This sub-circuit is tuned to block the 2MHz signal from being coupled to the 13MHz source. Inductor $L_5$ is coupled across input terminals 214A, 214B. The capacitors $C_7$, $C_6$ and $C_5$ are coupled in series from the input terminal 214A to an input 216A to the 13MHz tuning circuit 204. The inductors $L_4$ and $L_3$ are respectively coupled in parallel from the junction of capacitors $C_7$ and $C_6$ and capacitors $C_6$ and $C_5$. In one embodiment, the inductors $L_4$ and $L_5$ are about 2μH and inductor $L_3$ is about 1μH. The capacitors $C_6$ and $C_7$ are about 400pF and capacitor $L_5$ is about 800pF.

**[0019]** Second sub-circuit 204 comprises capacitor $C_3$, inductor $L_2$ and variable capacitor $C_4$. The variable capacitor $C_4$ is shunted across input terminals 216A, 216B from the generator isolation sub-circuit 206 and the inductor $L_2$ and capacitor $C_3$ are connected in series from the input terminals 216A and 216B to the common output terminal 212. In one embodiment, variable capacitor $C_4$ is nominally variable from about 400pF to about 1200pF, inductor $L_2$ is about 2.4μH, and capacitor $C_3$ is about 67pF.

**[0020]** Typically, in the current state of the art technology for impedance matching, either the series and shunt elements are varied, or the elements are fixed and the source frequency is varied to achieve an impedance match between a source and the load (*e.g.*, the plasma). Where the series and shunt elements are varied, the elements responsible for matching one of the source frequencies can impact the load impedance seen by the elements responsible for matching the other source frequency. For example, Figures 3A and 3B show how the tune space for 2MHz and 13MHz shifts when the other frequency's match elements are varied. In Figure 3A, the shunt components (*e.g.*, capacitors $C_1$ and $C_4$ in Figure 2) are shown to have little or no effect on the other frequency's tune space (as depicted by overlaying lines 302 and 304,

and 306 and 308). However, when the series component corresponding to one frequency source (*e.g.*, inductor $L_1$ and capacitor $C_2$ or inductor $L_2$ and capacitor $C_3$ in Figure 2) is varied, the tune space for the other frequency shifts. Figure 3B depicts the effect of varying the series component at 13MHz. When the 13MHz series component is varied, the 2MHz tune space shifts. This is shown by the shift in lines 306 and 308, which no longer overlap.

**[0021]** The design of the present invention, however, as discussed above with reference to Figures 1 and 2, results in a match tune space that can be varied by shunt component tuning without the undesirable side-effect on the other frequency's tune space. Consequently, the complimentary frequency tune space remains unaffected, and a zero reflected power tune space can be realized over a large impedance range.

**[0022]** For example, Figure 4 depicts a plot of the tune space seen using the matching circuit 108 of Figure 2. This configuration can be contained in either a fixed match condition, where the component values are set prior to a process run and the values are fixed for the entire run, or the circuit 108 can be implemented in a frequency/shunt autotune match configuration, where the frequency of the generator is tuned to establish the azimuthal tuning direction of the matching circuit and the variable shunts (capacitors $C_2$ and $C_4$) will set the radial tuning direction. These two tuning mechanisms (frequency tuning and shunt tuning) operate in perpendicular directions in the tune space and can independently tune to the optimal condition given the appropriate time response for an autotuning algorithm. As such, this form of tuning prevents unstable feedback between the two systems that may cause an un-tunable condition.

**[0023]** Examples of plasma enhanced semiconductor processing chambers that may be adapted to benefit from the present invention include, but are not limited to, the eMax™, MXP®, and ENABLER™ processing chambers, all available from Applied Materials, Inc. of Santa Clara, California. The eMax™ processing chamber is described in United States Patent No. 6,113,731, issued September 5, 2000 to Shan et al. The MXP® processing chamber is described in United States Patent No. 5,534,108, issued July 9, 1669 to Qian et al., and United States Patent No. 5,674,321, issued October 7, 1997 to Pu et al. The ENABLER™ processing chamber is described in United States Patent No.

6,528,751, issued March 4, 2003 to Hoffman et al. Each of these above-mentioned patents are hereby incorporated by reference in their entireties.

**[0024]** Figure 5 depicts a partial schematic, cross-section view of a capacitively coupled, plasma enhanced processing chamber 500 suitable for use with the present invention. In one embodiment, a process chamber 500 includes a grounded chamber body 502 and at least one coil segment 518 disposed proximate to the exterior of the chamber body 502. The process chamber 500 also includes a wafer support pedestal 516 disposed within the chamber body 502 and spaced apart from a gas inlet 532. The wafer support pedestal 516 comprises a cathode 527 and an electrostatic chuck 526 for retaining a substrate 514 beneath the gas inlet 532.

**[0025]** The electrostatic chuck 526 is driven by a DC power supply 520 to develop an electrostatic force that holds the substrate on the chuck surface. The cathode 527 is coupled to a pair of RF bias sources 104, 106 through a dual frequency, variable shunt matching circuit 108. The bias sources 104, 106 are generally capable of producing an RF signal having a frequency of from about 50kHz to about 14.2MHz and a power of between about 0 and about 5000Watts. The dual frequency, variable shunt matching circuit 108 matches the impedance of the sources 104, 106 to the plasma impedance. A single feed 114 couples energy from both sources to the support pedestal 516.

**[0026]** The gas inlet 532 may comprise one or more nozzles or a showerhead. The gas inlet 532 may comprise a plurality of gas distribution zones such that various gases – which, when ignited, form a plasma 510 – can be supplied to the chamber body 502 using a specific gas distribution gradient. The gas inlet 532 may form an upper electrode 528 that opposes the support pedestal 516.

**[0027]** In operation, a substrate 514 is disposed in the processing chamber 500 and held to the support pedestal 516 by the electrostatic chuck 526. A process gas is introduced into the chamber body 502 through the gas inlet 532 by the gas source 508. A vacuum pump, not shown, maintains the pressure inside the chamber body 502 at operating pressures – typically between about 10 mTorr to about 20 Torr.

[0028] The RF source 104 provides about 5000W of RF voltage at 13.56 MHz to the cathode 527 through the dual frequency, variable shunt matching circuit 108, thereby exciting the gas inside the chamber body 502 and forming a plasma 510. The RF source 106 provides about 5000W of RF voltage at a frequency of about 2 MHz to the cathode 527 through the dual frequency, variable shunt matching circuit 108. The RF source 106 provides bias power that both self-biases the substrate and modulates the plasma sheath. After a period of time, or the detection of a specific endpoint, the plasma is extinguished.

[0029] While the foregoing is directed to the illustrative embodiment of the present invention, other and further embodiments of the invention may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.